AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph [0002] with the following amended paragraph:

[0002] The use of bi-directional shift ~~registers~~ register stages for drive circuits in liquid crystal displays (LCD) to allow a ~~positive~~ forward or a reverse display image. By causing the image to be scanned in one direction a ~~positive~~ forward, normal or non-reverse image may be displayed. However, when the image is scanned in a second direction, a reversed image may be displayed. United States Patent (USP) No. 5,894,296, entitled "Bidirectional Signal Transmission Network and Bidirectional Signal Transfer Shift Register," issued April 13, 1999, to Maekawa, teaches the use of bidirectional shift register control circuits in the LCD displays. In this circuit, the input and output terminals of the shift register are connected in a manner to construct a multi-stage structure, having a forward route gate element interposed in a connection between the output terminals.

Please replace the paragraph [0003] with the following amended paragraph:

[0003] Figure 1a illustrates an exemplary conventional bi-directional shift register and control circuit. In this illustrative example, three shift register stages, represented as 110, 120, and 130, are shown serially connected through control circuits 115, 125, and 135, respectively. Shift registers stages 110, 120 and 130 conventionally are referred to, and referred to herein, as the (N-1), (N) and (N+1) stages of shift register circuit 100. This generalization of shift register 100 into (N-1), (N) and (N+1) elements is terminology recognized by those skilled in the art in that the operation of shift registers

is performed with regard to adjacent register elements. The generalization of shift register 100 is further appropriate as it would be understood that any number of registers may be electrically connected, physically or logically, to create a shifting device of any size.

Please replace the paragraph [0005] with the following amended paragraph:

[0005] Control lines CL_1 145 and CL_2 140 are used to set control circuits 115, 125, and 135 in a manner to direct the data in the shift register to be shifted in a ~~positive~~ forward or reverse direction. Typically control lines CL_1 145 and CL_2 140 are set to different values. When CL_1 145 is set to a high level, CL_2 140 is set to a low level to operate in a first direction and reversed operate in second direction. .

Please replace the paragraph [0006] with the following amended paragraph:

[0006] Figures 1b and 1c illustrate ~~positive~~ forward and reverse timing sequences of the shift register 100 shown in Figure 1a. Referring to Figure 1a, a pulse 116p output on output terminal 114 is provided as an input to control circuit 125, which is further provided to input terminal 122 of shift ~~register 120~~ register stage 120. Shift ~~register 120~~ register stage 120 then provides pulse 126p from output terminal 124 to input of control circuit 135. Control circuit 135 provides an input voltage to shift register 130 through input terminal 132. Shift register 130 then provides pulse 136p at output terminal 134. This progressive shifting of an initial pulse in a ~~positive~~ forward, i.e., "*p*," direction continues for each of the stages in the shift register device. Figure 1c illustrates a pulse

shifting sequence in a reverse, i.e., "*r*," direction for the shift register shown in Figure 1a. In this case, pulse 136r on output terminal 134 is input to control circuit 125, which then provides an input to ~~register 120~~ shift register stage 120. ~~Register 120~~ Shift register stage 120 generates pulse 126r on corresponding output line 124 that is applied as an input to control circuit 115. The process is repeated for each shift register stage in the shifting device.

Please replace the paragraph [0007] with the following amended paragraph:

[0007] Figure 2 illustrates a conventional control circuit representative of an N^{th} register stage, for example, control circuit 125 and shift ~~register 120~~ register stage 120. Within control circuit 125 are switches 210 and 220 that are operable to direct either the output of the N-1 stage, i.e., 116p, or the (N+1) stage, i.e., 136r, to input 122 of shift register stage 120. In this illustrated case, switches 210 and 220 are represented as n-type Field Effect Transistors (FETs). Control lines 140 and 145 are electrically connected to switches 220 and 210, respectively. In this case, when a high signal, e.g., V_{dd}, is applied to control line 145 and a low signal, e.g., V_{ss}, is applied to control line 140, switch 210 is closed and switch 220 remains open. An input from an (N-1) stage, e.g., pulse 116p, is provided to the input of shift register stage 120 and data is shifted from the (N-1) stage to an N^{th} stage. Alternatively, when a high signal is applied to control line 140 and a low signal is applied to control line 145, switch 210 remains open and switch 220 is closed. In this case, an input from the (N+1) stage, e.g., 136r, is provided to the input of shift register stage 120 and data is reverse shifted from the (N+1) stage to an N^{th} stage.

Please replace the paragraph [0008] with the following amended paragraph:

[0008] A problem with the conventional implementation is that it may suffer from a gate element leakage. For example, if gate element 220 has a sufficient voltage leakage between its source and drain terminals, i.e., it cannot be sufficiently turned off by the control signal on CL2, that under ~~positive~~ forward shifting operation with CL2 at low level, for example, the pulsed signal voltage '(N+1) out' may leak into the input terminal 122 of- the electrically adjacent N^{th} shift register stage and introduce an error.

Please replace the paragraph [00010] with the following amended paragraph:

[00010] A bi-directional shift register circuit comprising, a plurality of shift ~~registers~~ register stages, each having an input and an output terminal, and a bi-directional shift controller circuit associated with each of said shift ~~registers~~ register stages is disclosed. The bi-directional shift controller circuit comprises a first input connected to the output terminal of a first shift register ~~output terminal~~ stage and a second input connected to ~~output terminal~~ the output terminal of a second shift register ~~output terminal~~ stage. ~~means~~ Means to apply a first and a second control voltage, wherein said first and second control voltage are different, and a combinatorial circuit responsive to said first and second control voltages to apply an indication of an input received from either said first shift register stage or said second shift register stage to ~~said~~ a corresponding shift register input terminal. The combinatorial circuit configuration is that of a NOR gate or a NAND gate.

Please replace the paragraph [00019] with the following amended paragraph:

[00019] Figure 3a illustrates a first exemplary embodiment 300 of the present invention. In this first embodiment, shown as a NOR gate combinational logic circuit, first transistor ~~or device~~ 310 is electrically connected to a first control line, CL_1 145, and a second ~~device~~ transistor 325. Second ~~device~~ transistor 325 is electrically connected between first ~~device~~ transistor 310 and third ~~device~~ transistor 320. Third ~~device~~ transistor 320 is electrically connected to a known voltage, in this case, V_{dd}. A fourth ~~device~~ transistor 330 is electrically connected between a second control line CL_2 140 and an ~~output~~ input terminal ~~that may be electronically connected to a~~ 122 of shift register stage 120 ~~input terminal~~ through the drain terminal. ~~One~~ Drain terminal of the first ~~device~~ transistor 310 is further connected to the ~~output~~ drain terminal of the fourth ~~device~~ transistor 330 for subsequent connection to the input terminal 122 of shift ~~register 120~~ register stage 120. The gate terminals of the first and third ~~device~~ transistors 310, 320 are connected to an electrical means that enables a voltage '(N-1) out' 350 to be concurrently applied thereto. Similarly the gate terminals of the second and fourth ~~device~~ transistors 325, 330 are connected to a means that enables a voltage '(N+1) out' 360 to be concurrently applied thereto.

Please replace the paragraph [00020] with the following amended paragraph:

[00020] In this exemplary embodiment, an output of an (N-1) stage, referred to as voltage ~~'(N+1)~~ '(N-1)out', 350, is provided to the gates ~~nodes or~~ terminals of n-type

transistor 310 and to p-type transistor 320 at ~~electrical connection or~~ terminal 352. Similarly, an output of a (N+1) stage, referred to as voltage '(N+1) out' 360, is provided to the gate ~~nodes or~~ terminals of n-type transistor 330 and to p-type transistor 325 at ~~electrical connection or~~ terminal 362.

Please replace the paragraph [00021] with the following amended paragraph:

[00021] Source terminals of n-type transistor 310 and transistor 330 are electrically connected to control line CL_1 145 and CL_2 140, respectively. In the present invention, CL_1 145 and CL_2 140 are set to different voltage levels to operate NOR circuit 300 as either a bi-directional ~~positive~~ forward shifting control circuit or a bi-directional reverse shifting control circuit

Please replace the paragraph [00022] with the following amended paragraph:

[00022] Figure 3b illustrates a timing sequence for operation of NOR circuit 300 as a bi-directional ~~positive~~ forward shifting control circuit in accordance with the principles of the invention. In this case, control line CL_1 145 is set to a low voltage, V_{ss}, and control line CL_2 140 set to a high voltage, V_{dd}. When the voltages of both ' (N-1) out' 350, and '(N+1) out' 360, are at low level, n-type transistors 310 and 330 are turned off while the p-type transistors 320 and 325 are turned on. Voltage '(N) in' 121 is, thus, set at a high voltage, V_{dd}, as the only the path between ~~node~~ input terminal 122 of shift register stage 120 and the source terminal of transistor 320 is conducting.

Please replace the paragraph [00023] with the following amended paragraph:

[00023] However, when voltage ' (N-1) out' 350 is at high level, represented as pulse 354 and voltage '(N+1) out' 360 is at low level, n-type transistor 310 and the p-type transistor 325 are turned on while n-type transistor 330 and the p-type transistor 320 are turned off. In this case, only the path between terminal 122 and the source terminal of transistor 310 is conducting. Thus, voltage '(N) in' 121 at input terminal 122 is at a level of that of CL_1 145, which is V_{ss}. As voltage '(N) in' 121 is at a low voltage, represented as pulse 126p', it is inverted with regard to input pulse 354. On the other hand, when voltage ' (N-1) out' 350 is at low level and voltage '(N+1) out' 360 is at high level, n-type transistor 330 and the p-type transistor 320 are turned on while n-type transistor 310 and p-type transistor 325 are turned off. In this case, only the path between input terminal 122 of shift register stage 120 and the source terminal of transistor 330 is conducting. Thus, the voltage '(N) in' 121 at input terminal 122 remains substantially at a high level, i.e., V_{dd}. The pulsed signal '(N+1) out' is blocked away from triggering shift register stage (N) by the invented bi-directional circuit under ~~positive~~ forward shifting operation.

Please replace the paragraph [00024] with the following amended paragraph:

[00024] Referring now to Figure 1a, to explain the time shift in voltage '(N+1) out' 360, when shift register stage (N) 120 receives a pulsed signal at its input terminal 122, it will generate an output pulse '(N) out' with a timing shift of a clock width similar to that shown in Figure 1b as 126p. The output pulse '(N) out' is fed to bi-directional

circuits 115 and 135. Under ~~positive~~ forward shifting operation, bi-directional circuit 115 does not response to '(N) out' while bi-directional circuit 135 will generate a pulsed signal from '(N) out' in order to trigger next shift register stage (N+1). Similarly, after stage (N+1) receives a pulsed signal at its input terminal 132, it will generate a shifted output pulse '(N+1) out', similar to that shown in Figure 1b as 136p. The pulse of '(N+1) out' is provided to bi-directional circuit 125 and bi-directional circuit of subsequent stage (N+2) (not shown in Fig. 1a). As the process continuing, pulses are generated and sequentially shifted.

Please replace the paragraph [00025] with the following amended paragraph:

[00025] Operation of NOR circuit 300 as a bi-directional reverse shifting control circuit is more clearly shown with reference to Figure 3c. Figure 3c illustrates a timing sequence for operation of NOR circuit 300 as a bi-directional reverse shifting control circuit in accordance with the principles of the invention. In this case, control line CL_1 145 is set to a high voltage, V_{dd}, and control line CL_2 140 set to a low voltage, V_{ss}. When the voltages of both ' (N-1) out' 350, and '(N+1) out' 360, are at a low level, n-type transistors 330 and 310 are turned off, while p-type transistors 320 and 325- are turned on. Voltage '(N) in' 121 is, thus, set at a high voltage, V_{dd}, as the only the path between ~~node~~ input terminal 122 of shift register stage 120 and the source terminal of transistor 320 is conducting.

Please replace the paragraph [00027] with the following amended paragraph:

[00027] Figure 4a illustrates a second exemplary embodiment 400 of the present invention. In this second embodiment, shown as a NAND gate combinational logic circuit, the configuration ~~of each of the devices~~ is the same as that described with regard to Figure 3a and need not be repeated. In this embodiment, p-type transistors replace the n-type transistors and n-type transistors replace the p-type ~~devices~~ transistors shown in Figure 3a. Furthermore, the known voltage applied to third ~~devices~~ transistor 420 is set at a low voltage, V_{ss}.

Please replace the paragraph [00028] with the following amended paragraph:

[00028] In operation of this second embodiment of the invention, the inverse of the voltage output of an (N-1) stage, referred to as '(N-1)*out', 450, is provided to p-type transistor 410 and concurrently applied to n-type transistor 420 through ~~electrical connection~~ terminal 452. Similarly, the inverse or inverted voltage output of an (N+1) stage, referred to as '(N+1)* out', 460, is provided concurrently to p-type transistor 430 and to n-type transistor 425 through ~~electrical connection~~ terminal 462. Furthermore, source terminals of the p-type transistor 410 and transistor 430 are electrically connected to control line CL_1 145 and CL_2 140, respectively. As previously discussed, in the present invention CL_1 145 and CL_2 140 are set to different voltage levels in order to operate the NAND circuit as a bi-directional ~~positive~~ forward or reverse shifting control circuit.

Please replace the paragraph [00029] with the following amended paragraph:

[00029] Figure 4b illustrates a timing sequence for operation of NAND circuit 400 as a bi-directional ~~positive~~forward shifting control circuit in accordance with the principles of the invention. In this case, control line CL_1 145 is set to a high voltage, V_{dd}, and control line CL_2 140 set to a low voltage, V_{ss}. When the voltages of both '(N-1)*out' 450, and '(N+1)*out' 460, are at high level, p-type transistors 410 and 430 are turned off while the n-type transistors 420 and 425 are turned on. Voltage '(N) in', 121 is, thus, set at a low voltage, V_{ss}, as the only the path between ~~node~~ input terminal 122 of shift register stage 120 and the source terminal of transistor 420 is conducting.

Please replace the paragraph [00030] with the following amended paragraph:

[00030] However, when voltage '(N-1)*out' 450 is at low level, represented as inverted pulse 454, and voltage '(N+1)* out' out 460 is at high level p-type transistor 410 and the n-type transistor 425 are turned on while the p-type transistor 430 and the n-type transistor 420 are turned off. Voltage '(N) in' 121 is at a level of that of CL_1 145 which is V_{dd} as only the path between input terminal 122 of shift register stage 120 and source terminal of transistor 410 is conducting

Please replace the paragraph [00031] with the following amended paragraph:

[00031] Figure 4c illustrates a timing sequence for operation of NAND circuit 400 as a bi-directional reverse shifting control circuit in accordance with the principles of the invention. In this case, control line CL_1 145 is set to a low voltage, V_{ss}, and control line CL_2 140 set to a high voltage, V_{dd}. When '(N-1)*out' 450 is at high level and

'(N+1)*out' 460 is at low level, represented as inverse pulse 464, p-type transistor 430 and the n-type transistor 420 are turned on while the p-type transistor 410 and the n-type transistor 425 are turned off. In this case, voltage '(N) in' 121 is at a level of that of CL_2 144, i.e., V_{dd}, as only the path between input terminal 122 of shift register stage 120 and the source terminal of transistor 430 is conducting

Please replace the paragraph [00032] with the following amended paragraph:

[00032] When the voltages of both '(N-1)*out' 450, and '(N+1)*out' 460, are at high level, p-type transistors 410 and 430 are turned off while the n-type transistors 420 and 425 are turned on. Voltage (N) in 121 is, thus, set at a low voltage, V_{ss}, as only the path between ~~node~~ input terminal 122 of shift register stage 120 and the source terminal of transistor 420 is conducting.

Please replace the paragraph [00033] with the following amended paragraph:

[00033] Further, when voltage '(N+1)*out' 460 is at high level and voltage '(N-1)*out' 450 is at low level, represented as inverse pulse 454, n-type transistor 425 and p-type transistor 410 are turned on while the n-type transistor 420 and the p-type transistor 430 are turned off. In this case, the path between input terminal 122 of shift register stage 120 and the source terminal of transistor 410 is conducting so that the voltage '(N) in' 121 is substantially at a level of that of CL_1 145, which is V_{ss}. In this case, voltage (N) in 121 remains at its normally low level state.